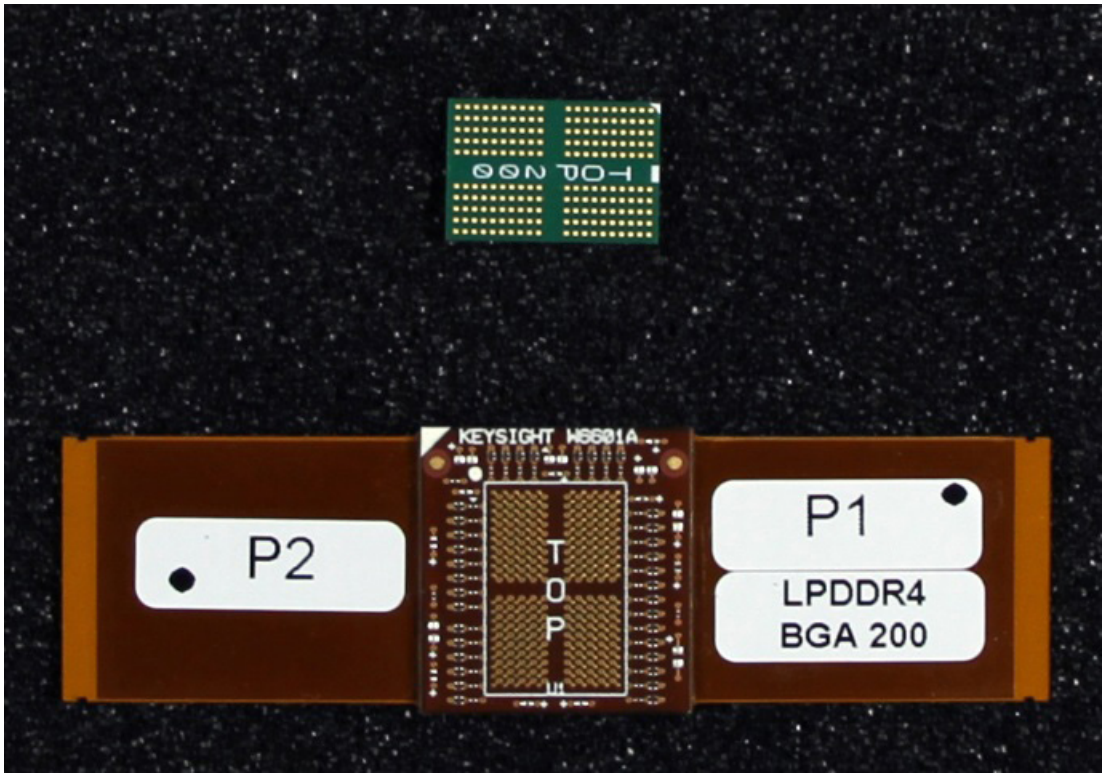
Keysight W6600A Series
LPDDR4 BGA Interposers

Data Sheet



KEYSIGHT TECHNOLOGIES

Introduction

The Keysight Technologies, Inc. W6600A Series LPDDR4 BGA interposers enable probing of embedded memory LPDDR4 DRAM from the ball grid array with Keysight U4164A logic analyzers.

The W6600A Series LPDDR4 BGA interposers are designed to take full advantage of quad sample state mode on U4164A modules with Option 02G, requiring only a single probe point for up to four samples at two different thresholds. W6600A Series BGA interposers are tested up to 3200 MT/s data rates.

The LPDDR4 BGA interposer advantage

Features	Benefits
Direct connection to the LPDDR4 BGA balls using a riser LPDDR4 200-ball DRAM at data rates up to and including 3.2 Gb/s with W6601A	Eliminates reflections from mid-bus probing methods. Also eliminates design time, prototype builds, and trace routing required to design in alternative probing methods
LPDDR4, decode, functional compliance and performance analysis using optional software tools	Accelerates navigation and insight of information captured in the logic analyzer trace via multiple different graphs and views of condensed analysis of LPDDR4 traces
APS (advanced probe pettings) to enable DQ (data) capture over 1866 Mb/s	Provides larger eyes to logic analyzer for accurate signal capture via internal logic analyzer comparator compensation
Leaded or lead-free solder supported	Works easily with all solder finishes. Designed to tolerate lead-free soldering temperature profiles
Contract manufactures available for those without the in-house expertise or facilities for soldering BGAs	Eliminates the need to develop BGA soldering expertise
Flexible “wings” with ZIF connectors	Ensures reliable connection to the ZIF probes. Enables placement of the probe cables around adjacent components. Minimizes the torque to the balls of the BGA

Table of Contents

W6600A Series LPDDR4 BGA Interposer Selection Guide

Memory family	Package	Data rates	Signal coverage	Use model	Keysight BGA interposer
LPDDR4	– 200-ball – 0.8 mm x 0.65 mm pitch – JEDEC MO-311 footprint with maximum DRAM package size of 10 mm x 15 mm can fit on top of W6601A without an additional (optional) riser or socket to provide clearance for the RC components	In excess of 3200 Mb/s	Command address: – All Channel A CA for Bank 0 and Bank 1 – No Channel B CA Control: -RESET – Channel A CKE0, CKE1, ODT, CS0, CS1, CK_A – No Channel B control Data: – DQ0_A, DQ7_A, DMI0_A, DQSt_A, DQ15_A, DQ8_A, DQ9_A, DMI1_A – DQ0_B, DQ1_B, DQ2_B, DQ3_B, DQ4_B, DQ7_B, DMI0_B – DQ8_B, DQ9_B, DQ10_B, DQ11_B, DQ12_B, DMI1_B	Debug and functional validation for LPDDR4 200-ball DRAM configured as single channel	W6601A
LPDDR4	– 200-ball – 0.8 mm x 0.65 mm pitch – JEDEC MO-311 footprint with maximum DRAM package size of 10 mm x 15 mm can fit on top of W6601A without an additional (optional) riser or socket to provide clearance for the RC components	In excess of 3200 Mb/s	Command address: – All Channel A CA for all banks – All Channel B CA for all banks Control: -RESET – Channel A CKE0, CKE1 [1], CKE2 [1], ODT, CS#0, CS#1, CS#2, CK_A – Channel B CKE0, CKE1 [1], CKE2 [1], ODT, CS#0, CS#1, CS#2, CK_B Data: – All Channel A DQ and DQSt – All Channel B DQ and DQSt	Debug and functional validation for LPDDR4 200-ball DRAM configured as either two individual 16 bit channels or a single 32 bit channel	W6602A

1. CKE1_A, CKE2_A, CKE1_B, CKE2_B, and RESET are routed to flying lead headers on the W6602A. For details, refer to the W6600A Series installation guide at: http://literature.cdn.keysight.com/litweb/pdf/W6600-97000.pdf

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ

LPDDR4 200-ball DRAM are dual x16 channel devices. They can be used as two single x16 channel devices or as a single x32 device.

The W6601A LPDDR4 200-ball BGA interposer is designed to satisfy functional debug and validation for LPDDR4 200-ball chip down systems using the DRAM as a single, 32-bit channel. If the DRAM is used as two channels, then the W6601A will only provide visibility to the logic analyzer for the CA and commands for Bank 0 and Bank 1 from Channel A.

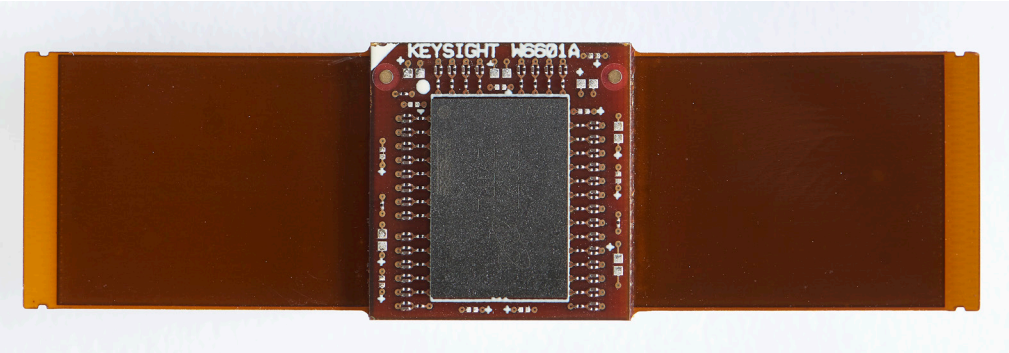


Figure 1. Top view of W6601A LPDDR4 200-ball BGA interposer with DRAM installed.

W6601A wings are designed to connect using one U4208A and one U4209A 61 pin ZIF probe/cables into a single U4164A logic analyzer.

Routing and cabling for the signals is single touch probing and is compatible with both Quad Sample State mode and Quarter Channel Timing modes of the U4164A logic analyzer. The exception is that Reset and CKE1 are NOT visible in Quarter Channel Timing mode, as those signals route into pods (3 and 7) and those pods loose the CK inputs when in Quarter Channel Timing mode. Quad Sample State mode is available only with Option -02G of the U4164A. Quarter Channel Timing mode is available in both Options -01G and -02G.

Software configurations for Quad Sample Timing mode and Quarter Channel Timing mode will be different as the labeling for Read /Write separation and rising /falling edges are not required in Timing modes.

At speeds under 2500 Mb/s, the W6601A can be used with dual-clock edge clocking and Dual-Sample mode instead of Quad Sample mode. Even in this reduced speed mode, it is recommended that the W6601A be used with a U4164A as the U4164A is the only LA with dual thresholds for Read/Write separation in Dual Sample mode.

Not all DQ are visible to the LA. This is due to routing limitations (even using single touch probing and the denser 61 pin ZIF). Refer to the W6601A pinout for the signals probed.

The U4208A connects to the left side of the W6601A and the U4209A connects to the right wing.

Notice: The U4208A and U4209A connect into the U4164A differently when used for the W6601A than they do for the W4640A Series DDR4 BGA interposers.

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ (Continued)

Technical characteristics

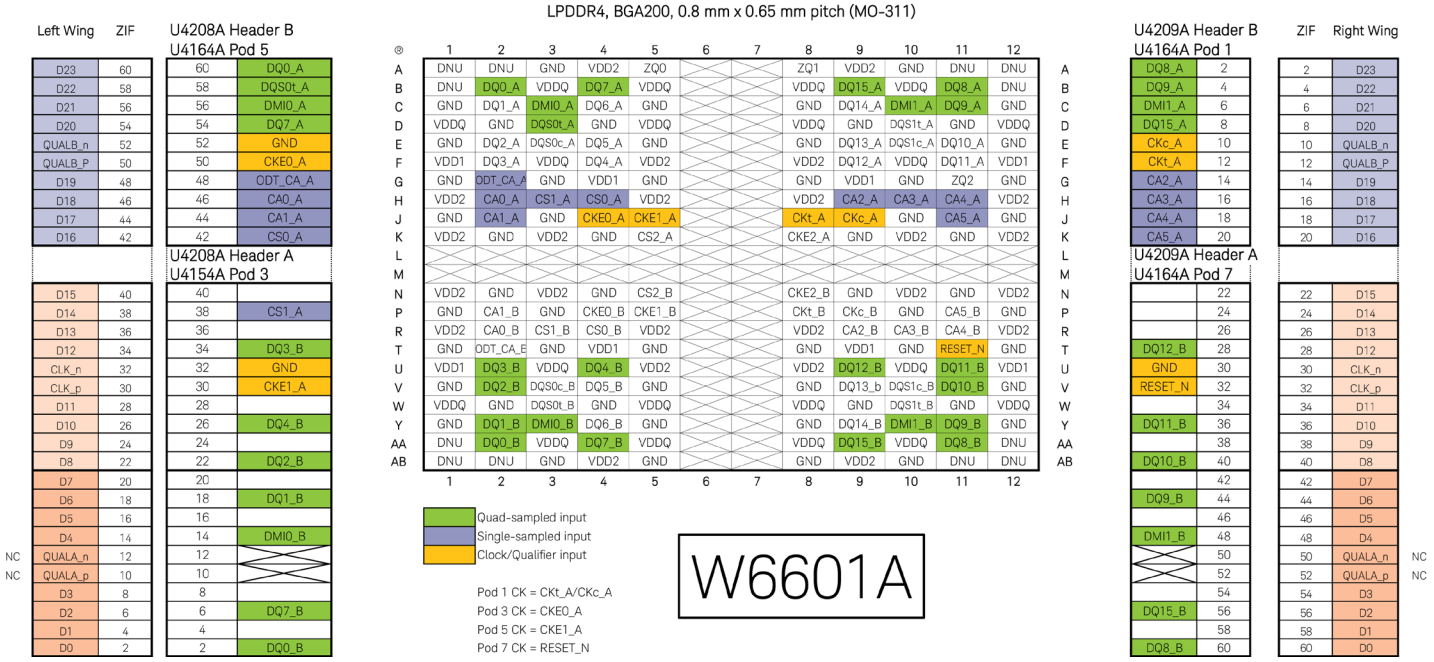
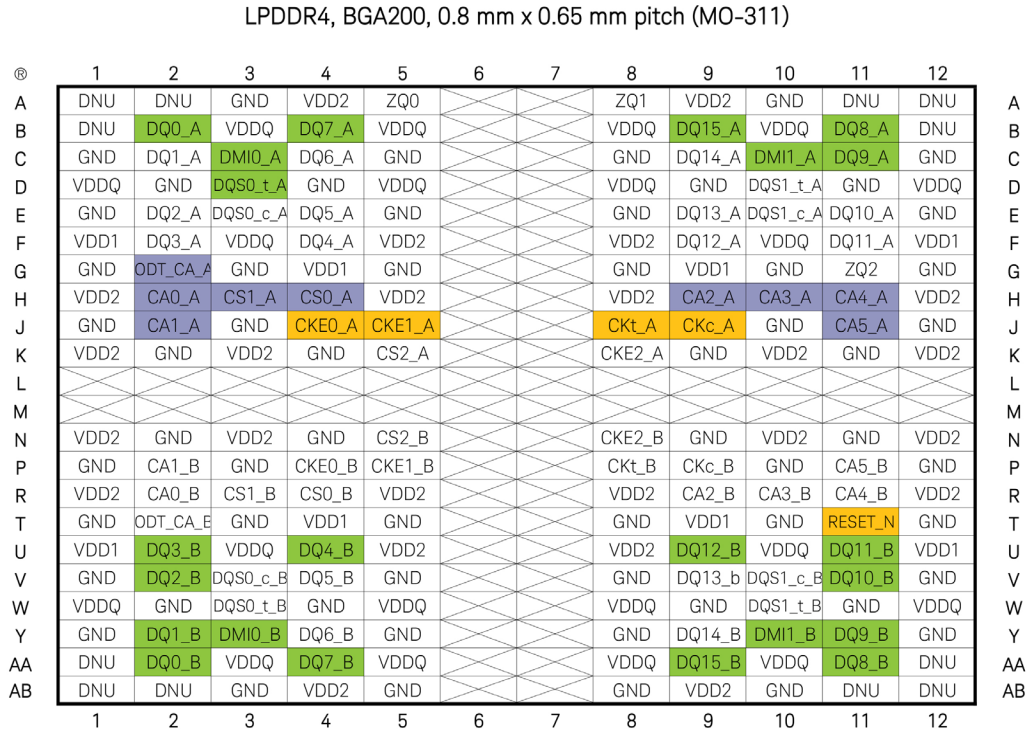


Figure 2. W6601A signals probed at 200-ball footprint and signal distribution through U4208A and U4209A ZIF probe/cables into the U4164A logic analyzer. Hardware connections are identical for all three W6601A default software configurations.



- DQ and DQS highlighted in 'green' are probed.
- CK and CKE highlighted in 'yellow' are probed.
- CA and ODT highlighted in 'indigo' are probed.

Figure 3. Signals routed from W6601A into logic analyzer.

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ (Continued)

Signal access

All signals, including power and ground signals, are passed between the system and memory chip.

LPDDR4 signal group logic analyzer signal access

Command/Address:
- All Channel A CA for Bank 0 and Bank 1
- No Channel B CA

Control and other signals:
- All for Channel A Bank 0 and Bank 1
- No Channel B control signals

Data:
- All except DQS0_c_A, DQS1_c_A, DQ1_A, DQ6_A, DQ14_A, DQ9_A, DQ2_A, DQ5_A, DQ13_A, DQ10_A, DQ3_A, DQ4_A, DQ12_A, DQ11_A, DQ2_B, DQ5_B, DQ13_B, DQ10_B, DQ1_B, DQ6_B, DQ14_B, DQ9_B

Power:
- DDR4 device power is not monitored by the logic analyzer
- Passed through the interposer through vias
- Locations for optional VDD and VDDQ bypass capacitors that can be used for power integrity measurements

W6601A series Interposers include separate ground, 1.1 V (VDD2/VDDQ), and 1.8 V (VDD1) planes. For additional installation information, refer to the W6600A Series installation guide at **http://literature.cdn.keysight.com/litweb/pdf/W6600-97000.pdf**.

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ (Continued)

Dimensional drawings

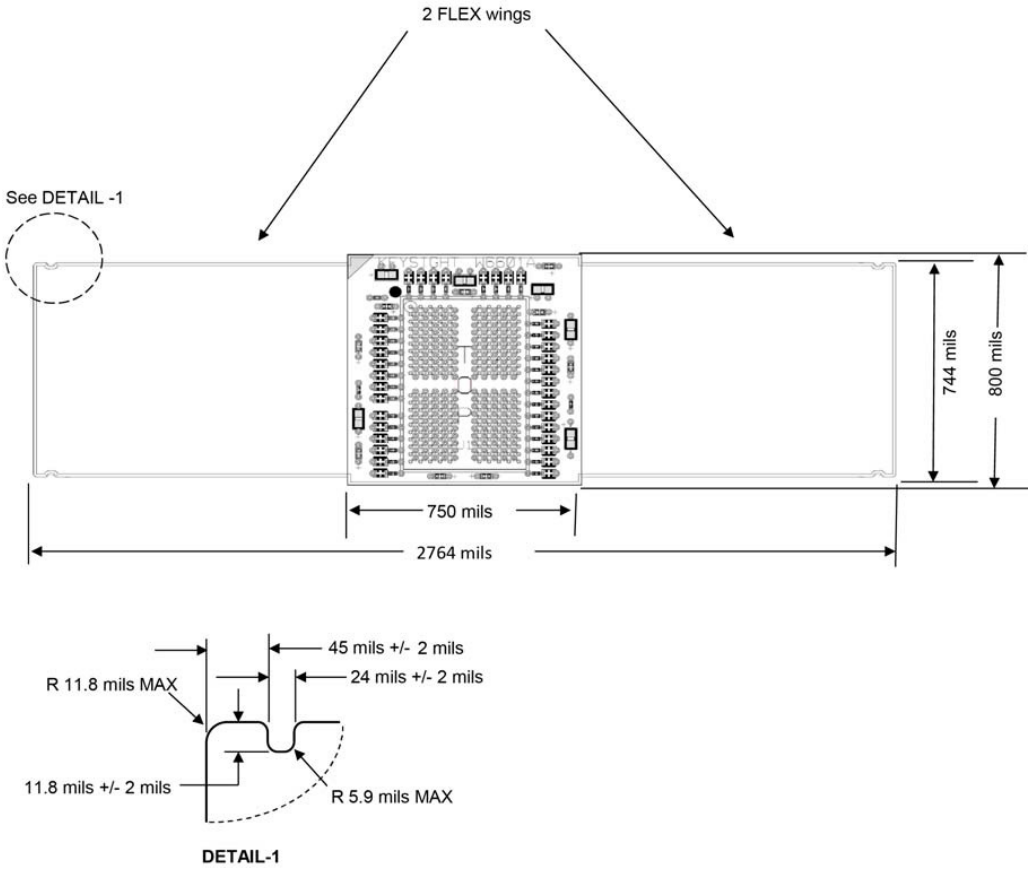


Figure 4a. W6601A top view.

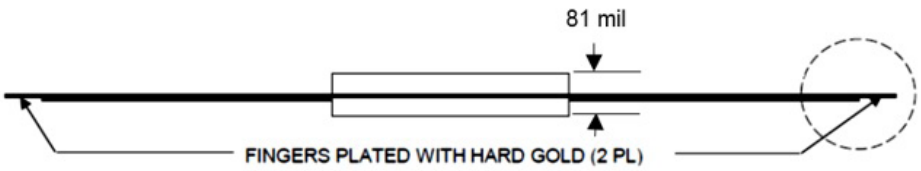
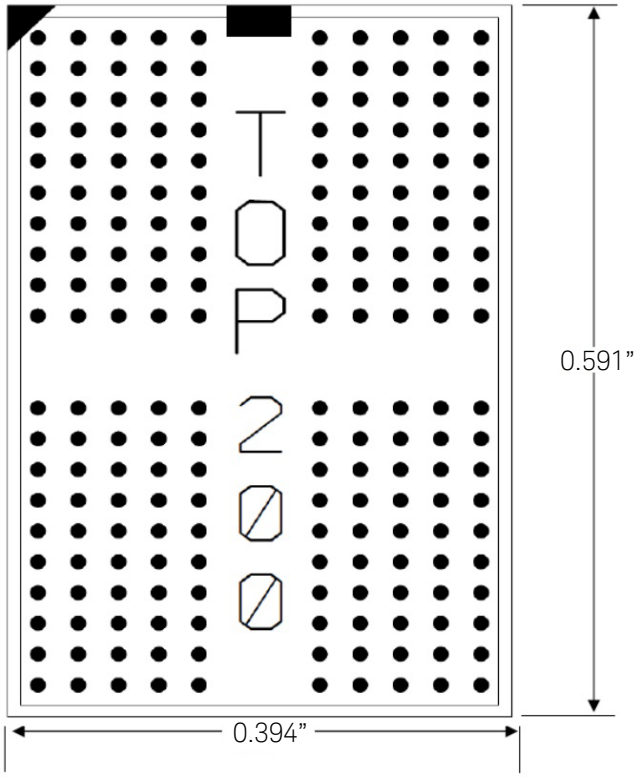


Figure 4b. W6601A side view.

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ (Continued)

Dimensional drawings (Continued)



Note: 0.067” thick

Figure 4c. LPDDR4 200-ball riser.

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ (Continued)

Images

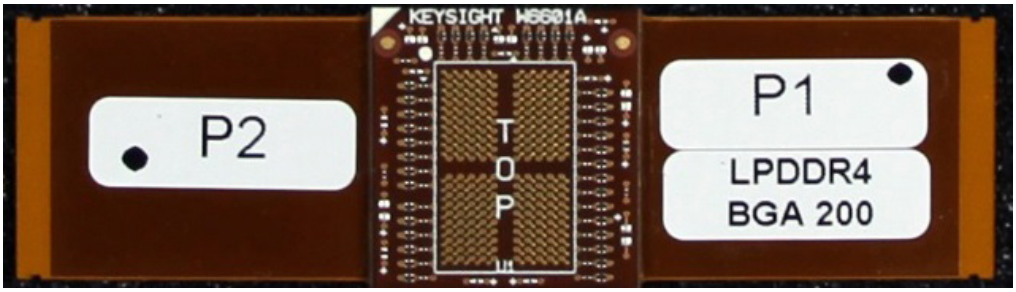


Figure 5. Top view of W6601A.

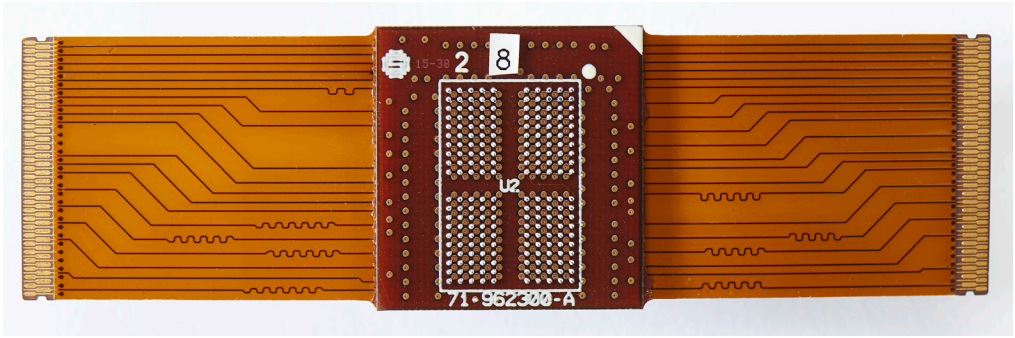


Figure 6. Bottom view of W6601A.

W6601A: LPDDR4 200 BGA Interposer 2-Wing, 3.2 Gb/s, CA Channel A, Partial DQ (Continued)

Connecting the U4208A and U4209A probe cables to a U4164A logic analyzer

In a W6601A interposer setup, you connect the U4208A and U4209A probe cable pods to U4164A logic analyzer pods per the mapping shown in the Table 1. (Hardware connections are valid for all three default software configurations.)

Table 1. Pod mapping

U4209A cable pods	**U4164A inputs**
Pod A	Pod 7
Pod B	Pod 1
U4208A cable pods	**U4164A inputs**
Pod A	Pod 3
Pod B	Pod 5

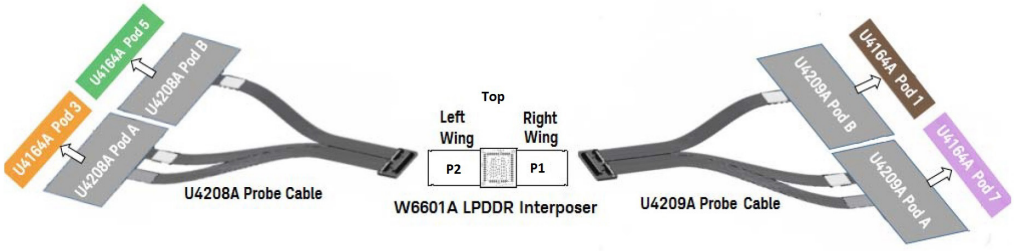


Figure 7. Connections between U4208A and U4209A probe cables and logic analyzer pods.

Note: U4208A and U4209A connect to the ZIF wings with the ZIF connector door closing against the top side of the wing.

W6602A: RC BGA Interposer, LPDDR4 200-Ball, Rigid, 3.2 Gb/s, CHA and CHB All DQ

The Keysight W6602A+U4207A passively monitors the LPDDR4 200 ball DRAM package. After tuning the Keysight analyzer, Command/Address bits can be reliably captured up to 3200 MT/s. At some data rates, the analyzer may not be able to provide an error-free capture of all DQ data bits.

LPDDR4 200-ball DRAM are dual x16 channel devices. They can be used as two single x16 channel devices or as a single x32 device. The W6602A LPDDR4 200-ball BGA interposer is designed to satisfy functional debug and validation for LPDDR4 200-ball chip down systems using the DRAM as either two single 16 bit channels or a single, 32-bit channel.

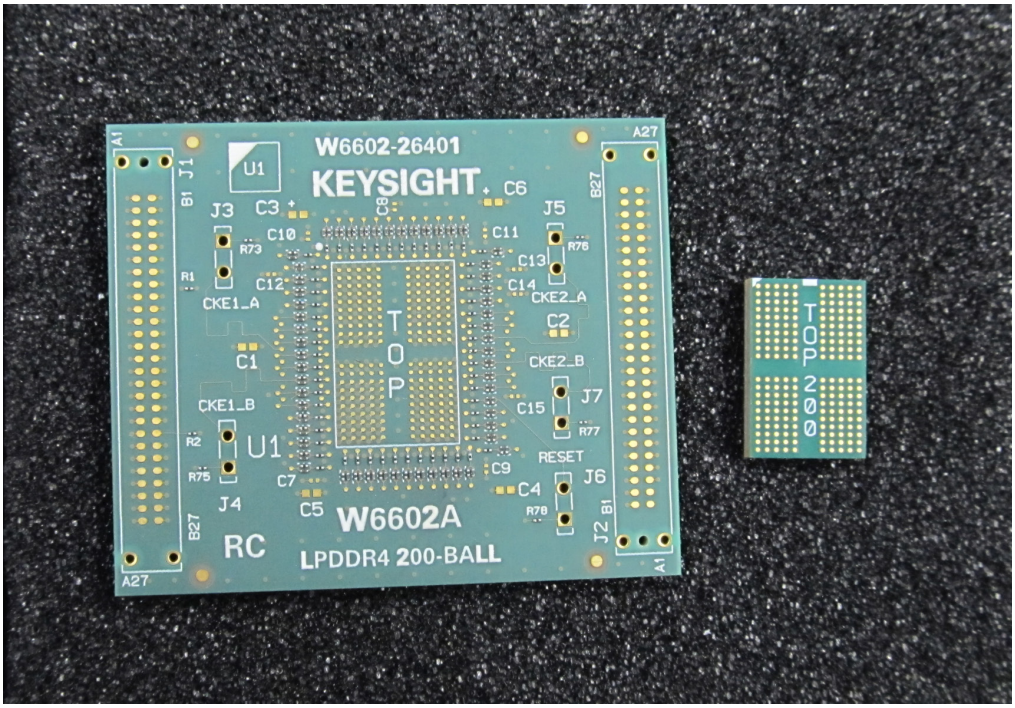


Figure 8. Top view of W6602A LPDDR4 200-ball, rigid RC BGA interposer and riser in shipping box.

Software configurations

The W6602A interposer can be used in the following seven logic analyzer software configurations; probing connections to the U4164A modules are unique for different configurations:

- 10 GHz timing mode
- CHA state mode 16 DQ under 2500MT/s (double edge clocking)
- CHA state mode 16 DQ over 2500MT/s (single edge clocking)
- CHA state mode 32 DQ under 2500MT/s (double edge clocking)
- CHA state mode 32 DQ over 2500MT/s (single edge clocking)
- CHB state mode 16 DQ under 2500MT/s (double edge clocking)
- CHB state mode 16 DQ over 2500MT/s (single edge clocking)

This interposer effectively utilizes the single touch probing and quad sampling features of the U4164A logic analyzer module, thereby allowing you to probe LPDDR4 DQ signals above 2.5 Gb/s without double probe load. (In quad sampling, four samples are captured per clock edge at two different thresholds. Two samples are taken at each threshold.) The Quad Sample State mode is only available with the U4164A-02G licensed speed grade option.

W6602A: RC BGA Interposer, LPDDR4 200-Ball, Rigid, 3.2 Gb/s, CHA and CHB All DQ (Continued)

Technical characteristics

The diagram below illustrates the pinout of the two connectorless footprints - J1 and J2 on top of a W6602A interposer.

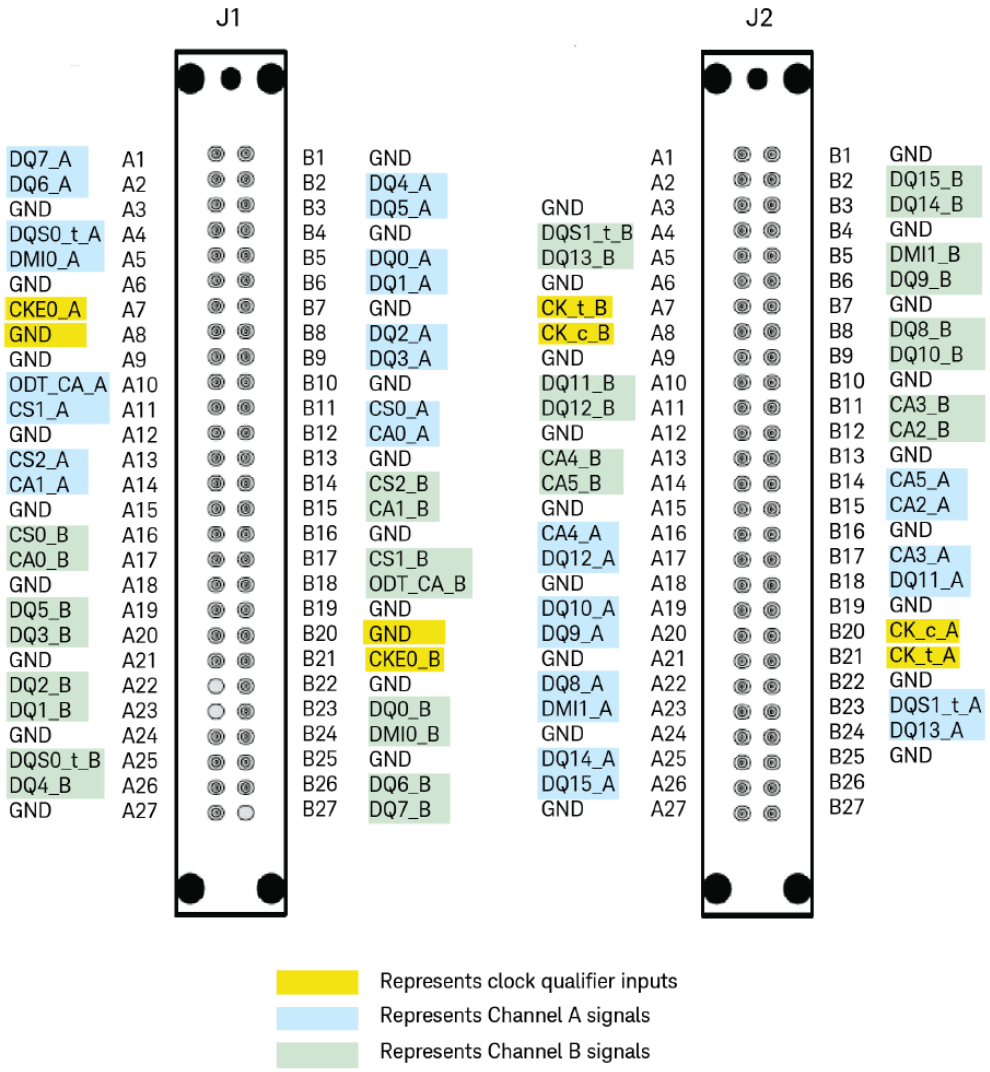


Figure 9. W6602A signals probed at 200-ball footprint and signal distribution through two U4207A probe/cables into the U4164A logic analyzer. CKE1_A, CKE2_A, CKE1_B, CKE2_B, and RESET are routed to flying lead headers on the W6602A. For details, refer to the W6600A Series installation guide at: http://literature.cdn.keysight.com/litweb/pdf/W6600-97000.pdf

W6602A: RC BGA Interposer, LPDDR4 200-Ball, Rigid, 3.2 Gb/s, CHA and CHB All DQ (Continued)

Signal access

•	1	2	3	4	5	6	7	8	9	10	11	12	
A	DNU	DNU	GND	VDD2	ZQ0			ZQ1	VDD2	GND	DNU	DNU	A
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU	B
C	GND	DQ1_A	DMI0_A	DQ6_A	GND			GND	DQ14_A	DMI1_A	DQ9_A	GND	C
D	VDDQ	GND	DQS0_t_A	GND	VDDQ			VDDQ	GND	DQS1_t_A	GND	VDDQ	D
E	GND	DQ2_A	DQS0_c_A	DQ5_A	GND			GND	DQ13_A	DQS1_c_A	DQ10_A	GND	E
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1	F
G	GND	ODT_CA_A	GND	VDD1	GND			GND	VDD1	GND	ZQ2	GND	G
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2	H
J	GND	CA1_A	GND	CKE0_A	CKE1_A			CK_t_A	CK_c_A	GND	CA5_A	GND	J
K	VDD2	GND	VDD2	GND	CS2_A			CKE2_A	GND	VDD2	GND	VDD2	K
L													L
M													M
N	VDD2	GND	VDD2	GND	CS2_B			CKE2_B	GND	VDD2	GND	VDD2	N
P	GND	CA1_B	GND	CKE0_B	CKE1_B			CK_t_B	CK_c_B	GND	CA5_B	GND	P
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2	R
T	GND	ODT_CA_B	GND	VDD1	GND			GND	VDD1	GND	RESET_N	GND	T
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1	U
V	GND	DQ2_B	DQS0_c_B	DQ5_B	GND			GND	DQ13_B	DQS1_c_B	DQ10_B	GND	V
W	VDDQ	GND	DQS0_t_B	GND	VDDQ			VDDQ	GND	DQS1_t_B	GND	VDDQ	W
Y	GND	DQ1_B	DMI0_B	DQ6_B	GND			GND	DQ14_B	DMI1_B	DQ9_B	GND	Y
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU	AA
AB	DNU	DNU	GND	VDD2	GND			GND	VDD2	GND	DNU	DNU	AB
	1	2	3	4	5	6	7	8	9	10	11	12	

Clocks are highlighted in yellow

Channel A signals are highlighted in blue

Channel B signals are highlighted in green

Signals not probed are highlighted in red

Figure 10. Signals routed from W6602A for logic analyzer access.

All signals, including power and ground signals, are passed between the system and memory chip.

W6602A: RC BGA Interposer, LPDDR4 200-Ball, Rigid, 3.2 Gb/s, CHA and CHB All DQ (Continued)

LPDDR4 signal group logic analyzer signal access

Command/address:

- All Channel A CA
- All Channel B CA

Control and other signals:

- All for Channel A
- All for Channel B

Data:

- All DQ and DQSt for Channel A and Channel B

Power:

The W6600A Series interposers include separate ground, 1.1 V (VDD2/VDDQ), and 1.8 V (VDD1) planes and have locations for optional VDD and VDDQ bypass capacitors that can be used for power integrity measurements. For details, refer to the W6600A Series installation guide at: http://literature.cdn.keysight.com/litweb/pdf/W6600-97000.pdf

Signals not probed by the logic analyzer:

The following signals are omitted from the logic analyzer connections for the W6602A interposer.

Interposer	Signal name
W6602A	DQS0_c_A
	DQS1_c_A
	DQS0_c_B
	DQS1_c_B

Mechanical Considerations

Dimensional drawings

W6602A interposer dimensions

The following figure shows the dimensions of a W6602A LPDDR4 BGA interposer.

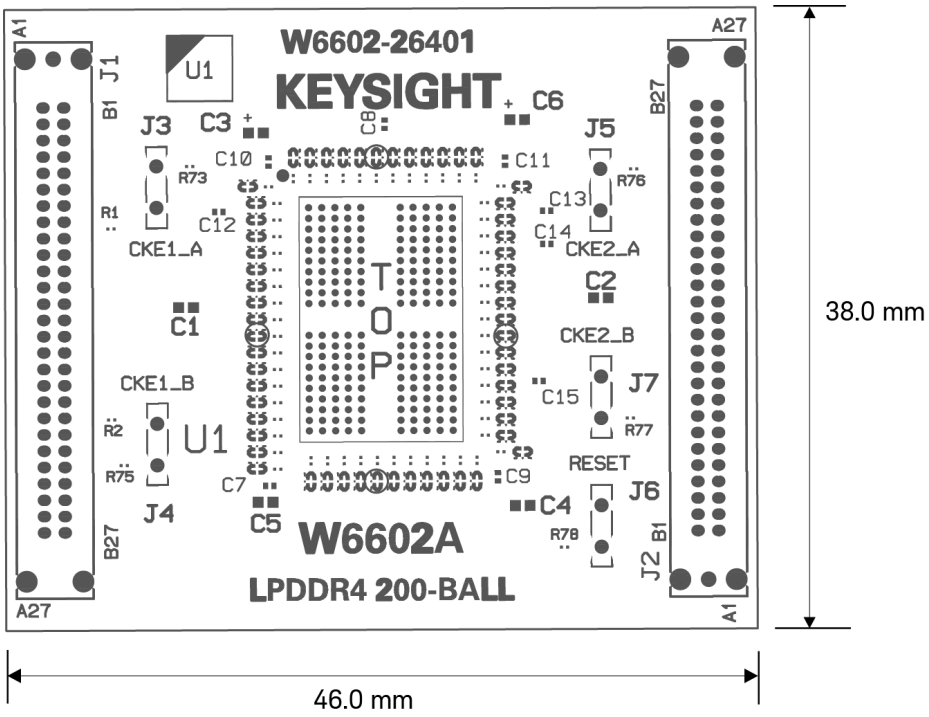


Figure 11. Dimensions of a W6602A interposer (top view). W6602A thickness is .067".

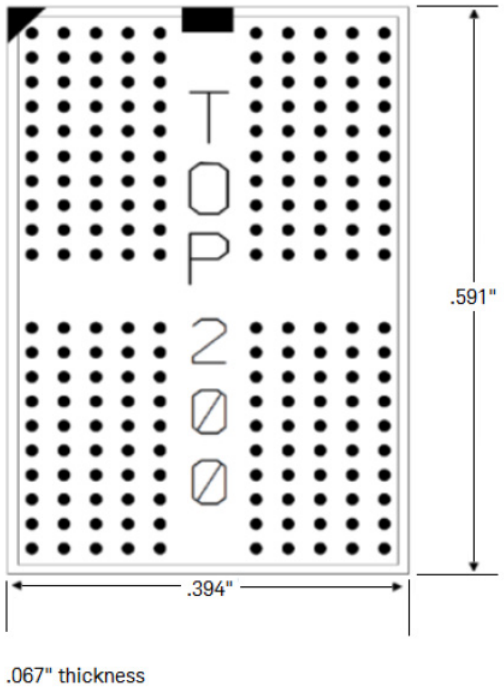


Figure 12. LPDDR4 200-ball riser. Dimensions in inches.

Mechanical Considerations (Continued)

Figure 13. Top view of W6602A LPDDR4 200-ball, rigid RC BGA interposer and riser.

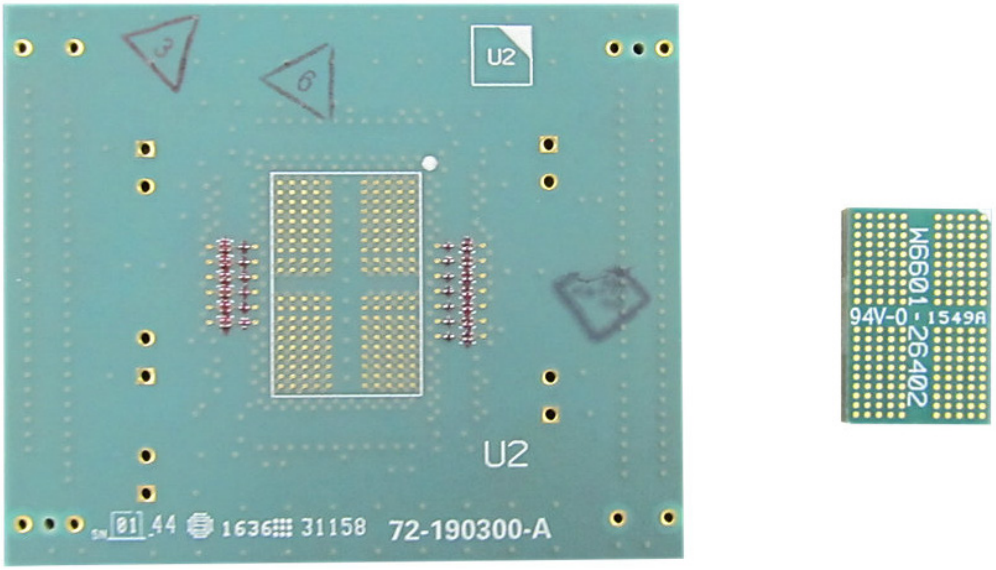


Figure 14. Bottom view of W6602A LPDDR4 200-ball, rigid RC BGA interposer and riser.

Mechanical Considerations (Continued)

Connecting the U4207A probe cables to a U4164A logic analyzer

In a W6602A interposer setup, connect the U4207A probe cable headers to U4164A logic analyzer pods per the mapping shown the following diagrams. (Hardware connections are unique for different software configurations.)

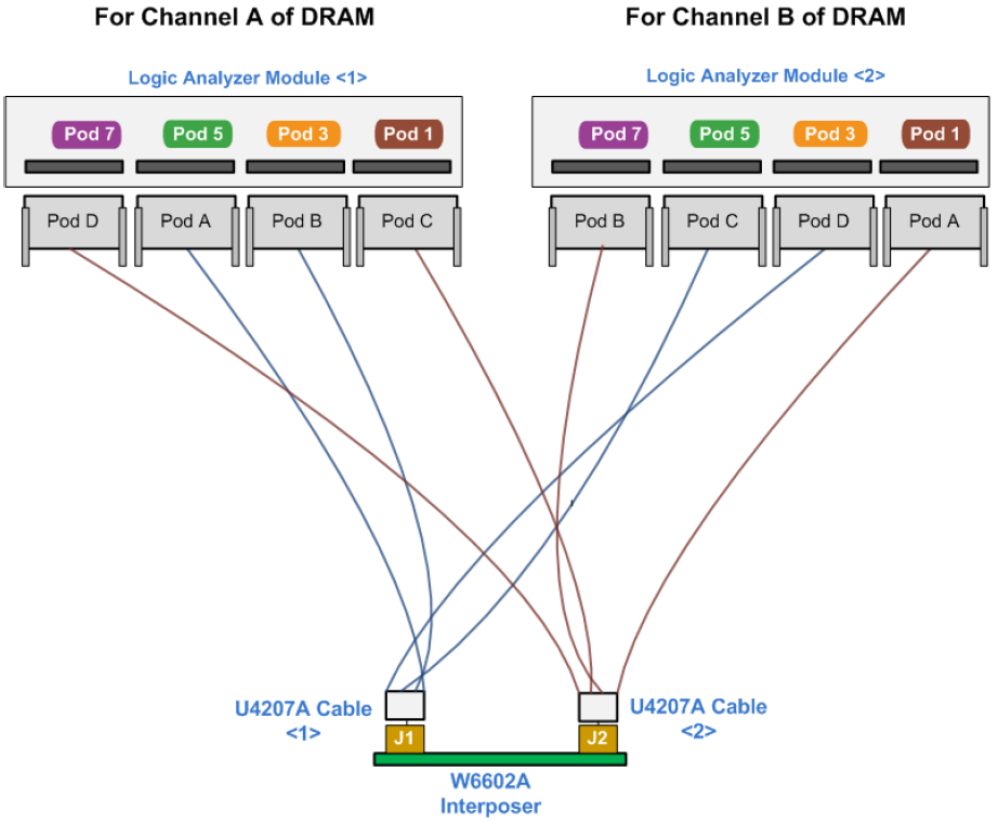


Figure 15. Connections between U4207A probe cables and logic analyzer pods for channel A and channel B 16 DQ configurations.

Mechanical Considerations (Continued)

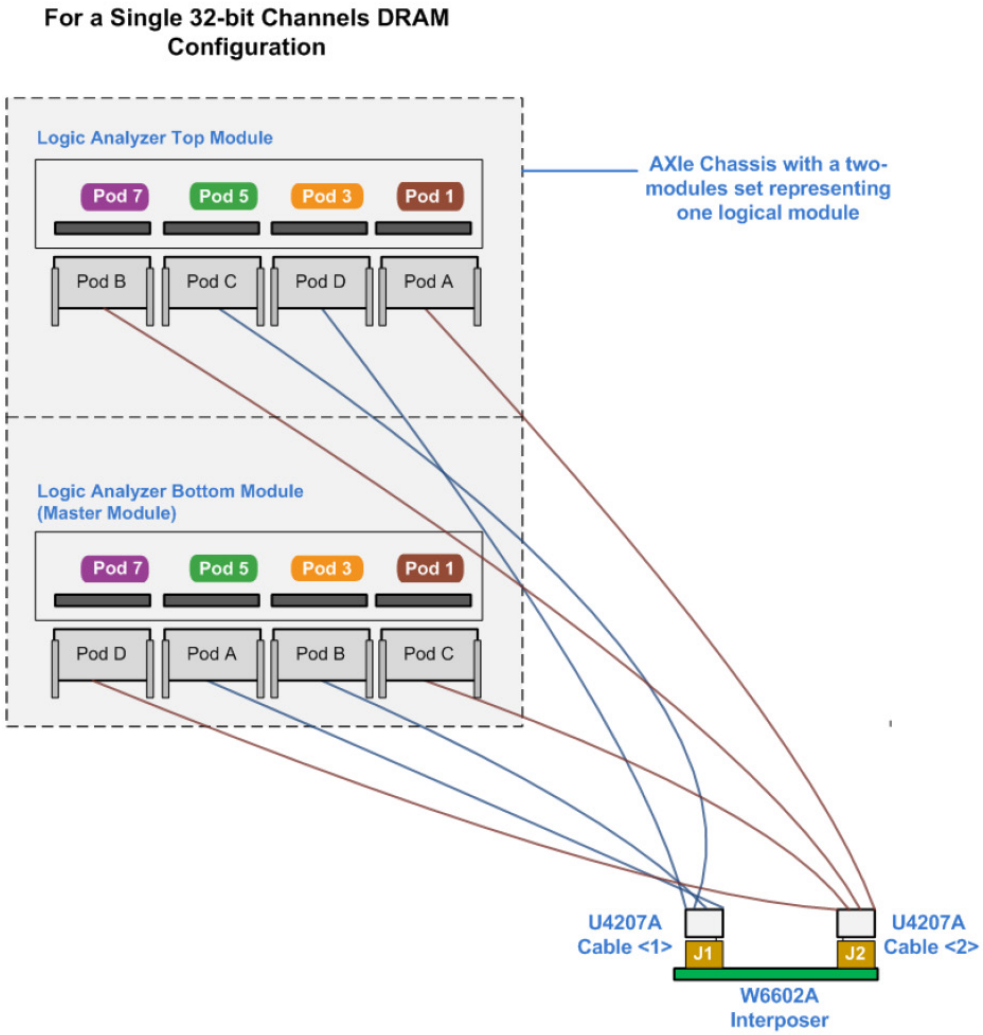


Figure 16. Connections between U4207A probe cables and logic analyzer pods for channel A 32 DQ and 10 GHz timing mode configurations.

Software

Default configurations for the W6600A Series interposers are included in the standard B4661A memory analysis software package. The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

B4661A standard software features

- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers. There are three default SW configurations for the W6601A:
  - 10 GHz Timing mode
  - State mode under 2500 Mb/s (double edge clocking)
  - State mode over 2500 Mb/s (single edge clocking)
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

The Keysight B4661A memory analysis software offers a suite of viewers and tools that include the industry's first protocol compliance violation testing capability across speed changes, a condensed traffic overview for rapid navigation to areas of interest in the logic analyzer trace, powerful performance analysis graphics, and DDR and LPDDR decoders. With the B4661A memory analysis software and a Keysight logic analyzer 1, users can monitor DDR3/4 or LPDDR2/3/4 systems to debug, improve performance, and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.

B4661A software options

- DDR decoder with physical address trigger tool
- LPDDR decoder with physical address trigger tool for LPDDR/2/3
- DDR and LPDDR compliance violation analysis toolset
- Post-process compliance violation analysis
- Real-time compliance violation analysis
- DDR3/4 and LPDDR2/3/4 performance analysis

DDR eye finder and eye scan software

DDR eye scan results of LPDDR4 signals gives you qualitative insight for all signals relative to each other. LPDDR4 signals are scanned in groups (Clock, CS#, ADD&Command, READ DQ/DQS, and WRITE DQ/DQS).

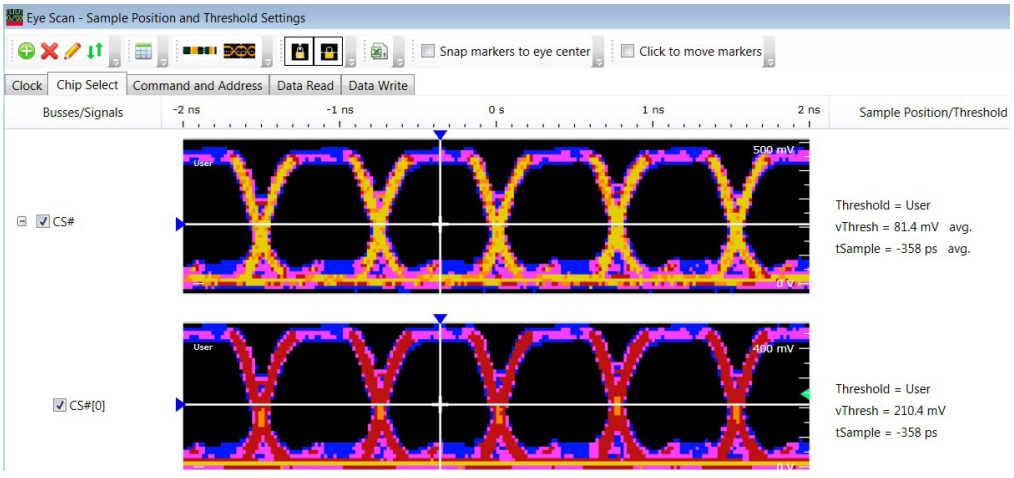


Figure 17. Eyescan of CS# shows large clean eyes.

Software (Continued)

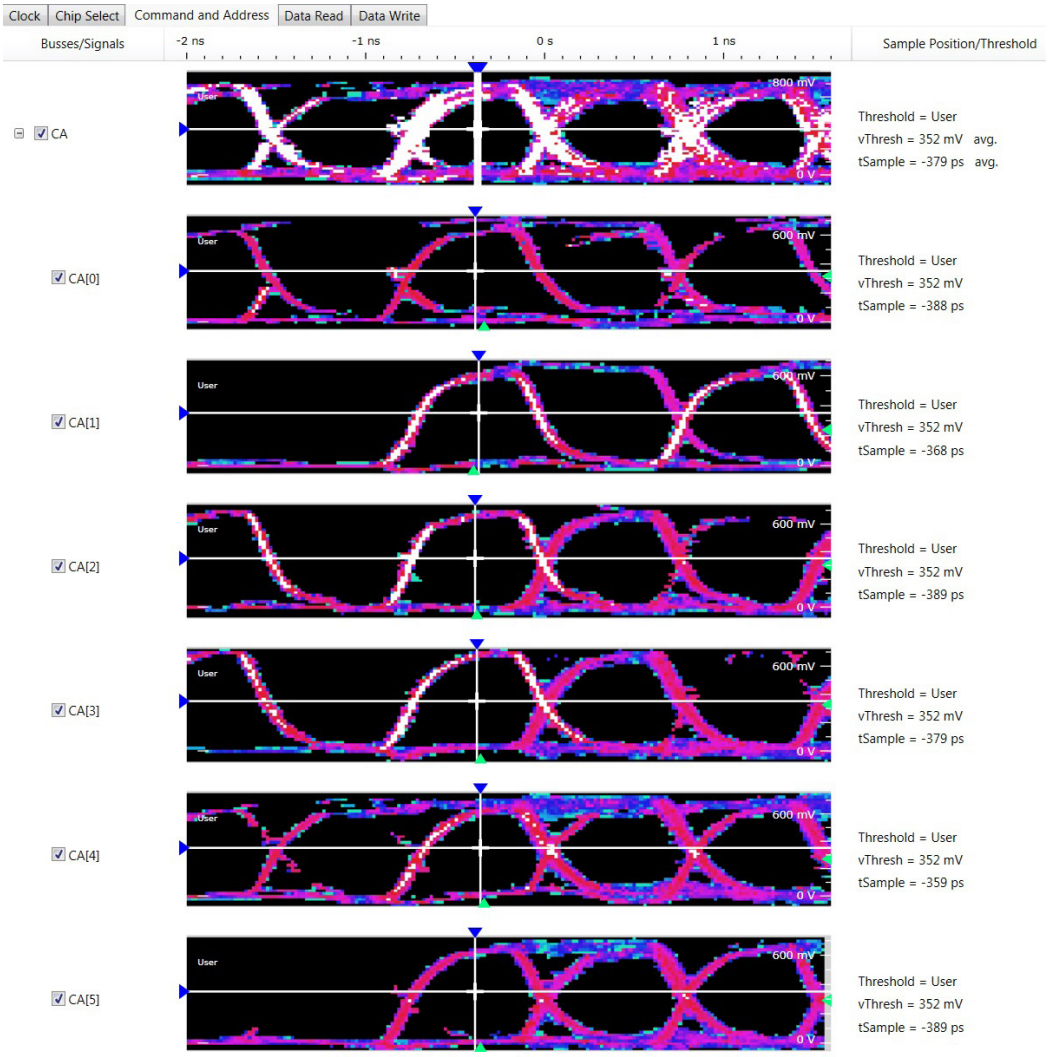


Figure 18. CA eye scans also show large open eyes. Light traffic shows up as incomplete lines in the CA scans.

Software (Continued)

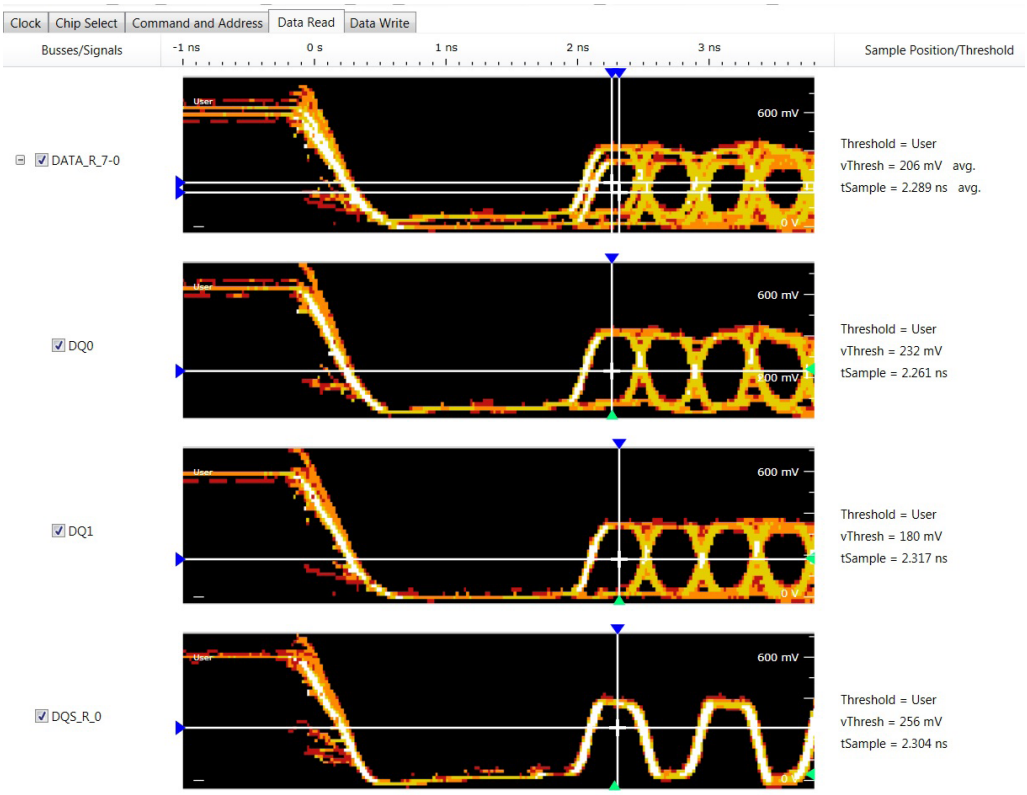


Figure 19. Read eye scans show the DQ traces are floating high when not preparing for a burst. Then the DQ and DQS are driven low prior to the burst. Note that the signal swing during the burst is only 400 mV to 10 mV. (Not unusual for LPDDR4, actually, this is a large swing for LPDDR4.)

Software (Continued)

Write signal trace eye scans

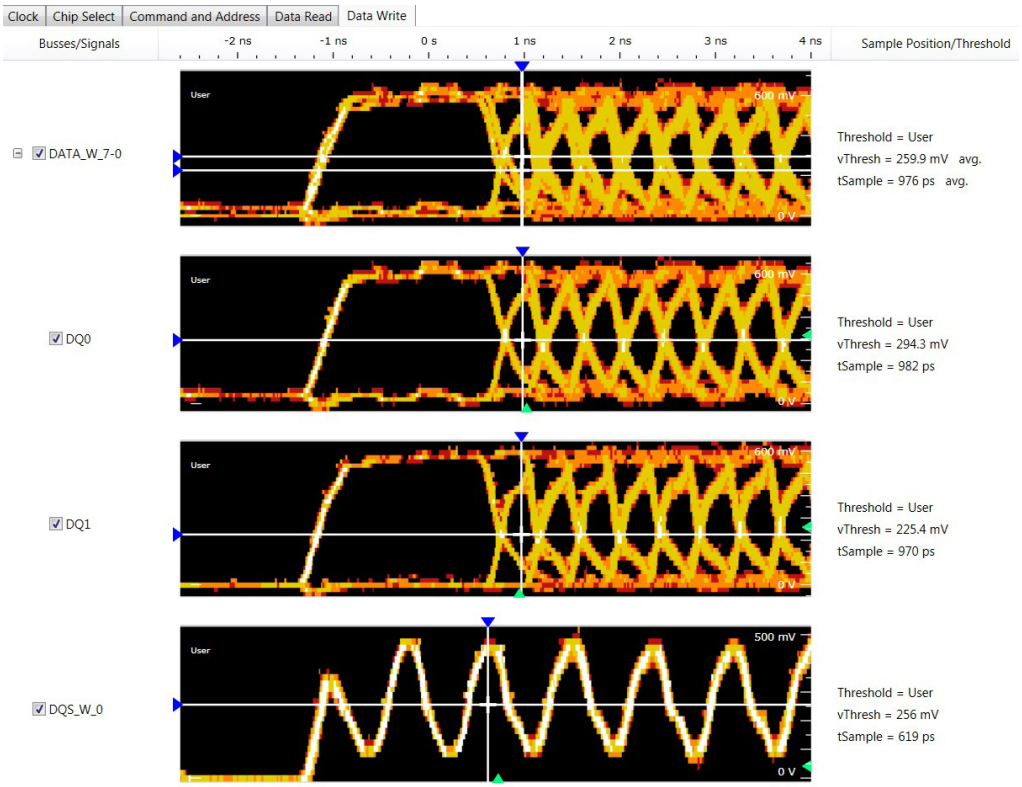


Figure 20. The LPDDR4 system has two DQS pulses for the Write preamble (per the LPDDR4 specification). No data is transferred during the Preamble. It is not unusual for the preamble pulse(s) to be shorter than the DQS pulses (edges that drive DQ transfer).

Software (Continued)

Optional software

Accelerate LPDDR4 analysis and debug using the B4661A memory analysis software with the W6601A LPDDR4 200-ball BGA interposer, U4208A and U4209A ZIF probe/cables, and U4164A logic analyzer.

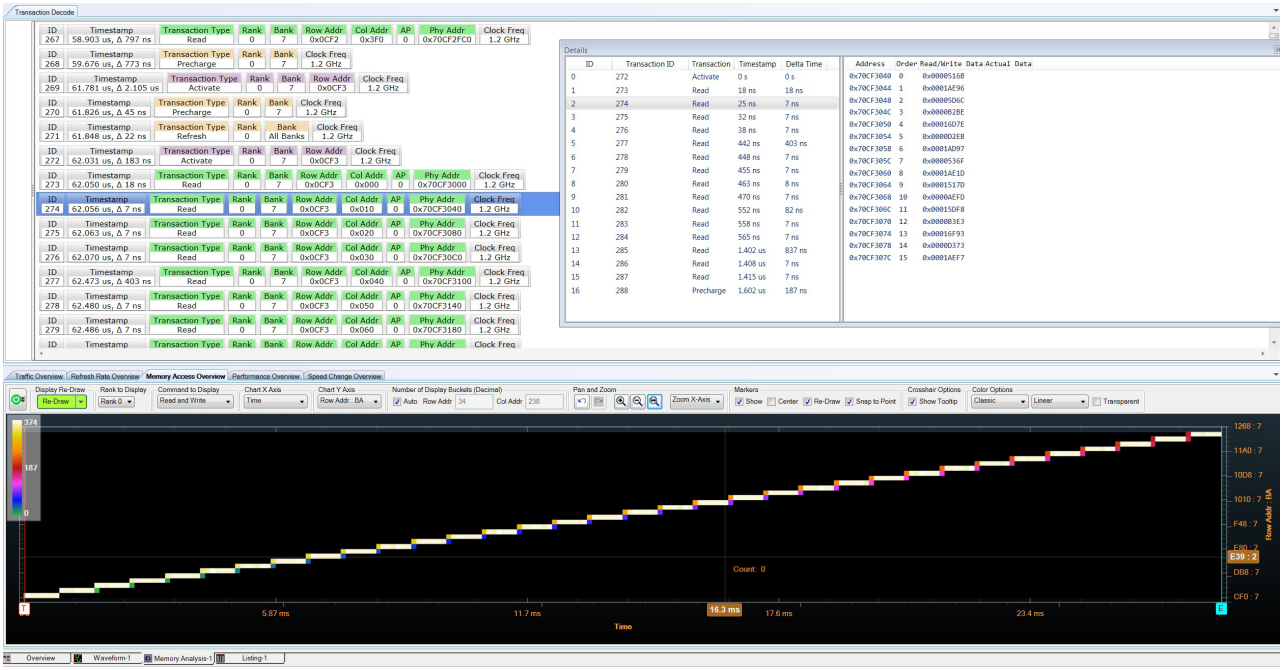


Figure 21. B4661A Option -4FP/TP/NP transaction decode, memory access overview graph and details window.

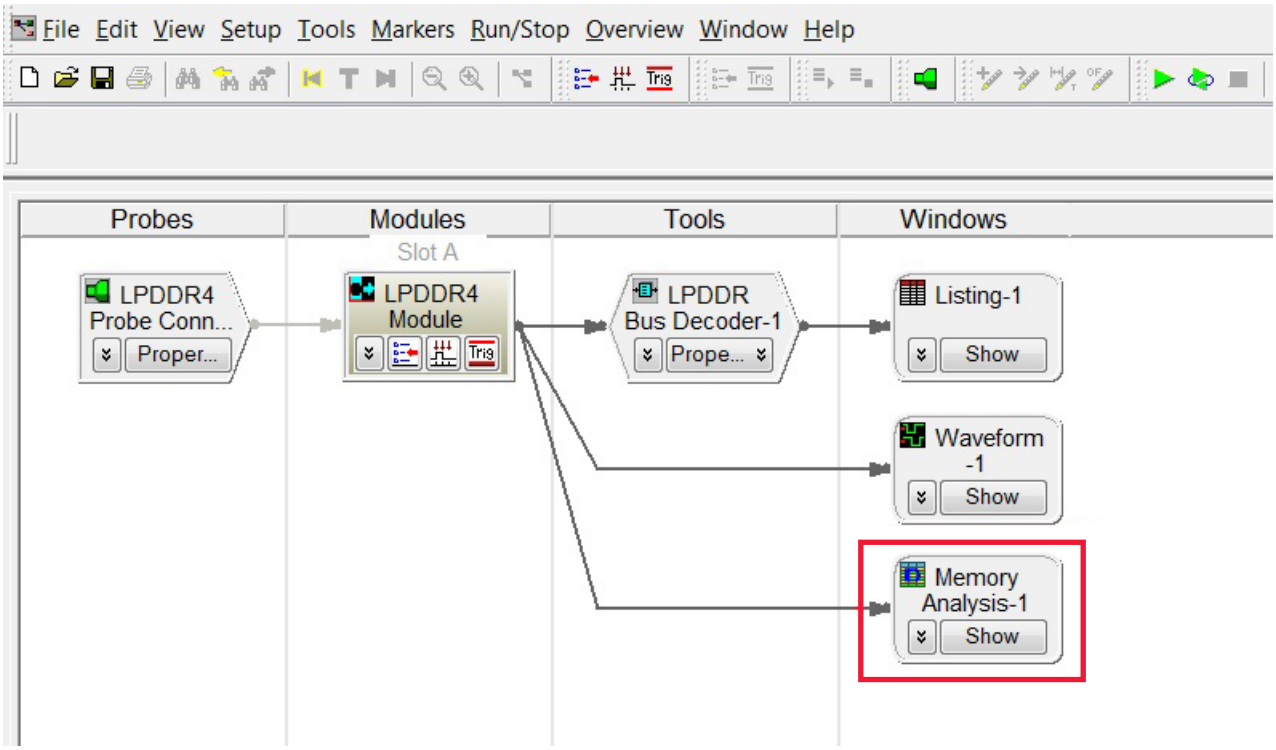


Figure 22. The memory analysis window is the B4661A -4FP/NP/TP option (performance analysis). All tabs in the Memory Analysis Window are dockable and can be moved around for user viewing preference.

Software (Continued)

Benefits of the B4661A performance analysis transaction decoder and traffic overview:

- Condensed view of all command activity in the trace
  - Including details of rank/bank, row, Col, BA, physical ADD, and clock frequency
- Enables rapid navigation of the trace
  - Click, scroll, or jump to commands of interest
  - Pan/zoom on chart of command activity
  - Place or jump to markers (markers are global across all windows/views)
- Users can rapidly notice variations in charts of the command activity that either make sense or do not

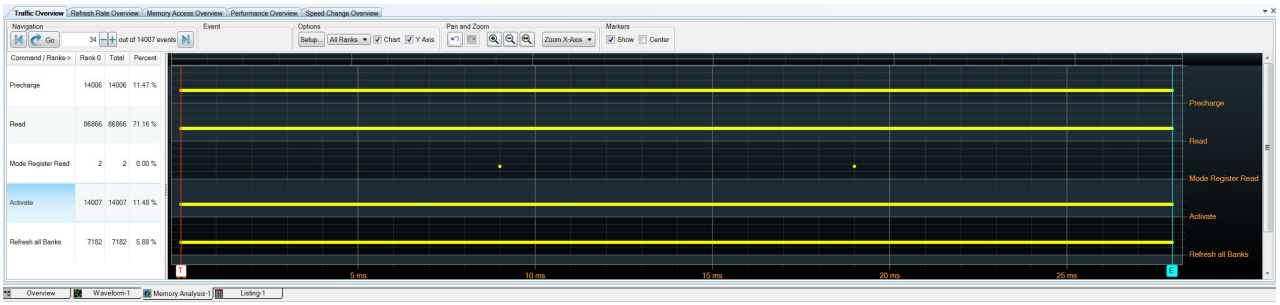


Figure 23. Traffic overview with graph. Notice that when you zoom in on the traffic overview graph you can see individual commands. In this trace, when all Ranks is selected, you only see one color (yellow) for Rank 0 as it is a single rank trace capture.

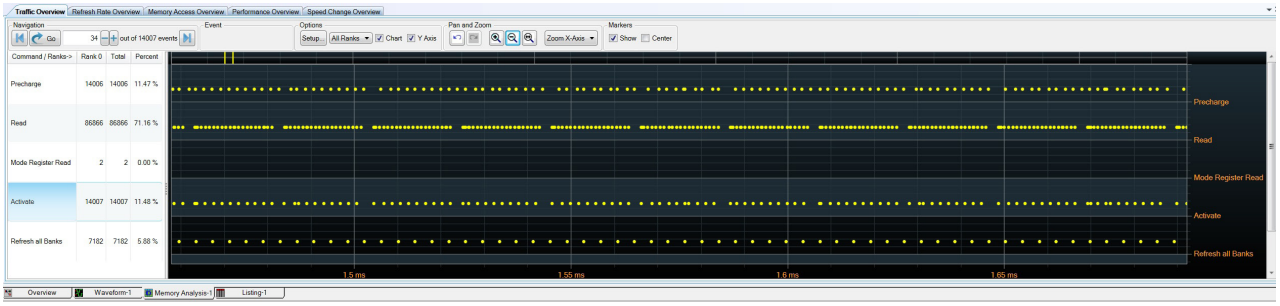


Figure 24. Zoom into details of command activity using Traffic Overview graph.

Details

ID	Transaction ID	Transaction	Timestamp	Delta Time
0	272	Activate	0 s	0 s
1	273	Read	18 ns	18 ns
2	274	Read	25 ns	7 ns
3	275	Read	32 ns	7 ns
4	276	Read	38 ns	7 ns
5	277	Read	442 ns	403 ns
6	278	Read	448 ns	7 ns
7	279	Read	455 ns	7 ns
8	280	Read	463 ns	8 ns
9	281	Read	470 ns	7 ns
10	282	Read	552 ns	82 ns
11	283	Read	558 ns	7 ns
12	284	Read	565 ns	7 ns
13	285	Read	1.402 us	837 ns
14	286	Read	1.408 us	7 ns
15	287	Read	1.415 us	7 ns
16	288	Precharge	1.602 us	187 ns

Address	Order	Read/Write Data	Actual Data
0x70CF3040	0	0x0000516B	
0x70CF3044	1	0x0001AE96	
0x70CF3048	2	0x00005D6C	
0x70CF304C	3	0x0000B2BE	
0x70CF3050	4	0x00016D7E	
0x70CF3054	5	0x0000D2EB	
0x70CF3058	6	0x0001AD97	
0x70CF305C	7	0x0000536F	
0x70CF3060	8	0x0001AE1D	
0x70CF3064	9	0x0001517D	
0x70CF3068	10	0x0000AEFD	
0x70CF306C	11	0x00015DF8	
0x70CF3070	12	0x0000B3E3	
0x70CF3074	13	0x00016F93	
0x70CF3078	14	0x0000D373	
0x70CF307C	15	0x0001AEF7	

Figure 25. Details tab available using B4661A -4FP/NP/TP performance analysis option.

Software (Continued)

The Details tab provides additional information on commands:

DDR/LPDDR DRAM banks must be activated (opening a “page” or “row”) prior to any Read/ Write activity to that bank/row. When the memory controller needs to access a different row address on the bank, a Precharge is issued to “close” the “page”.

The all associated Activates, Reads, Writes, and Precharges are displayed together on the left side of the Details tab. This is important information for debug and performance optimization of a system. (Page violations can result in corrupt data, and extra opening and closing of pages, which takes time and slows system performance.)

On the left side of the Details tab, you will see the data associated with any Read or Write command selected.

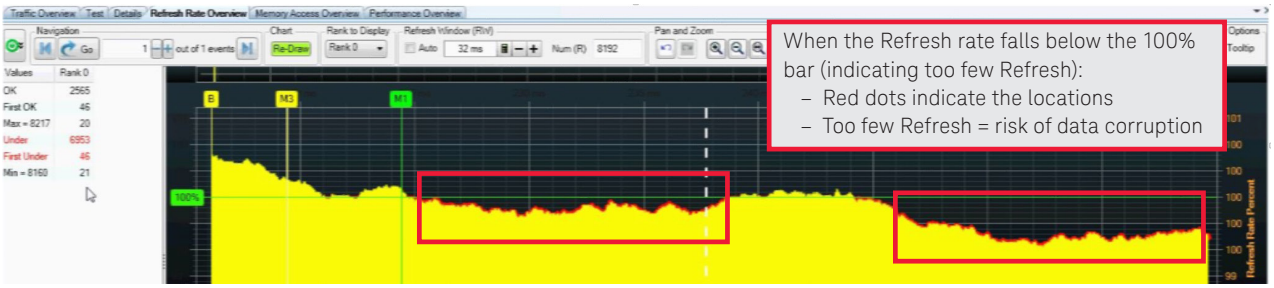


Figure 26. Refresh rate window.

Refresh rate overview

The refresh rate overview is an industry first. Analyzing a rolling 32 ms (adjustable) window of refresh activity to provide a percentage result for the minimum number of Refreshes required (also adjustable). This new analysis view is particularly suited to viewing the unique LPDDR4 refresh window. Deep traces, usually 128 M or deeper are required for meaningful refresh rate displays.

The Memory Access Overview allows the user to select different X & Y variables to view the entire Memory space accessed in the trace and to pan and zoom around the address space.

Time on the X and either BA:ROW or Row:BA are particularly insightful for highlighting “hot spots” of excessive activates to a particular Blank/Row address at a specific time. This can help users determine if particular memory tests or stimulus are possibly stressing Row Hammer. (Row hammer is a situation where internal Rows on any specific bank inside the DRAM are victims of cross talk from surrounding Rows in the bank.)

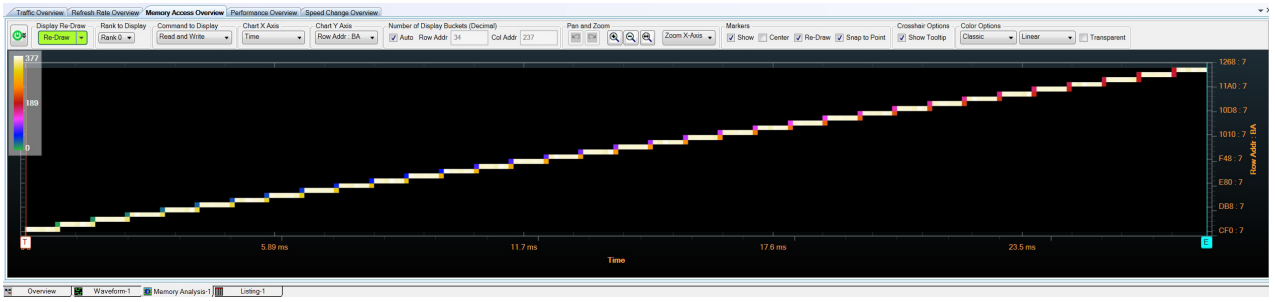


Figure 27. In Memory Access Overview set for Time Vs. RowAdd:BA, the system under test was steping through row addresses to individual banks. In this view, users can zoom in and re-draw to see more detail for a specific time.

Software (Continued)

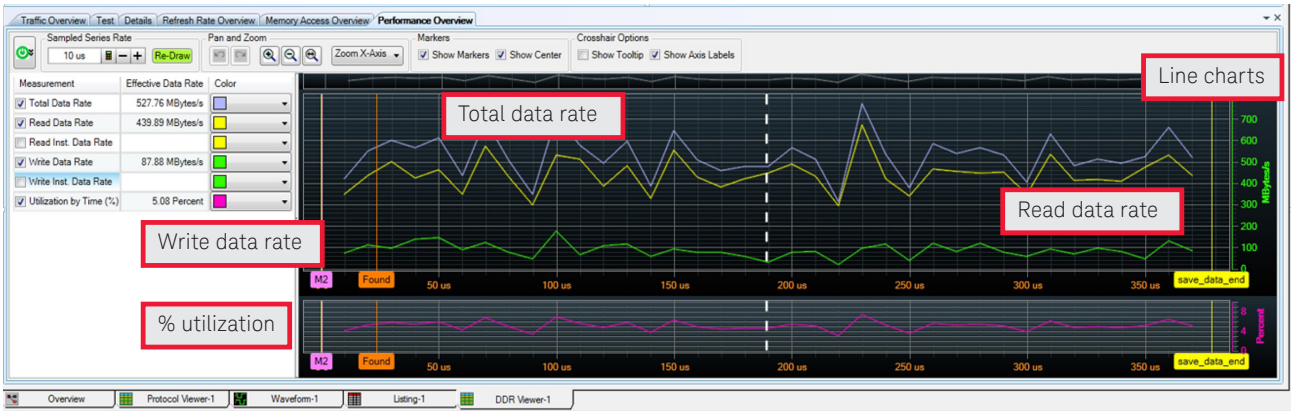


Figure 28. Performance analysis overview. B4661A Option -4FP/NP/TP provides data rate performance and percent utilization analysis and graphs.

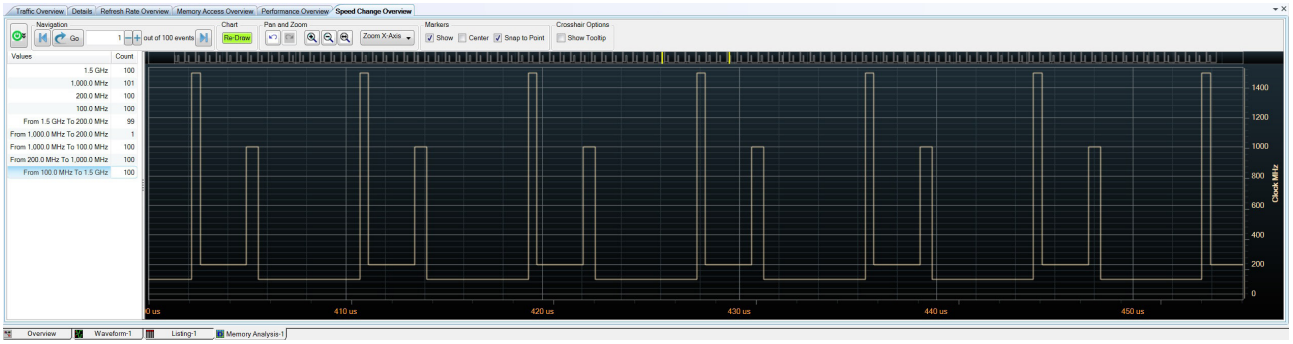


Figure 29. Clock frequency overview is provided in B4661A Option -4FP/NP/TP.

Clock frequency overview is very interesting to users with systems that are changing frequency. LPDDR systems can be aggressive at changing clock frequencies to conserve power.

DDR and LPDDR compliance violation analysis tool (B4661A-3FP/TP/NP)

The DDR and LPDDR compliance violation analysis toolset provides two tools under one license: post-process and real-time compliance violation tools. Both compliance tools cover DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, LPDDR3, and LPDDR4.

Key features of both the post-process and real-time compliance violation tools:

- Test compliance violations across speed changes using the post-process compliance violation tool
- Identify DDR/2/3/4 or LPDDR/2/3/4 state machine, protocol compliance, and protocol level bus cycle timing violations using either post-process or real-time tools
- Save time with automated real-time DDR2/3/4 or LPDDR2/3/4 protocol compliance measurements and trace captures using the real-time compliance violation analysis tool
- Edit parameters of the DDR/LPDDR standard preset tests easily using the enhanced parameter editing interface for both post-process and real-time tools

Software (Continued)

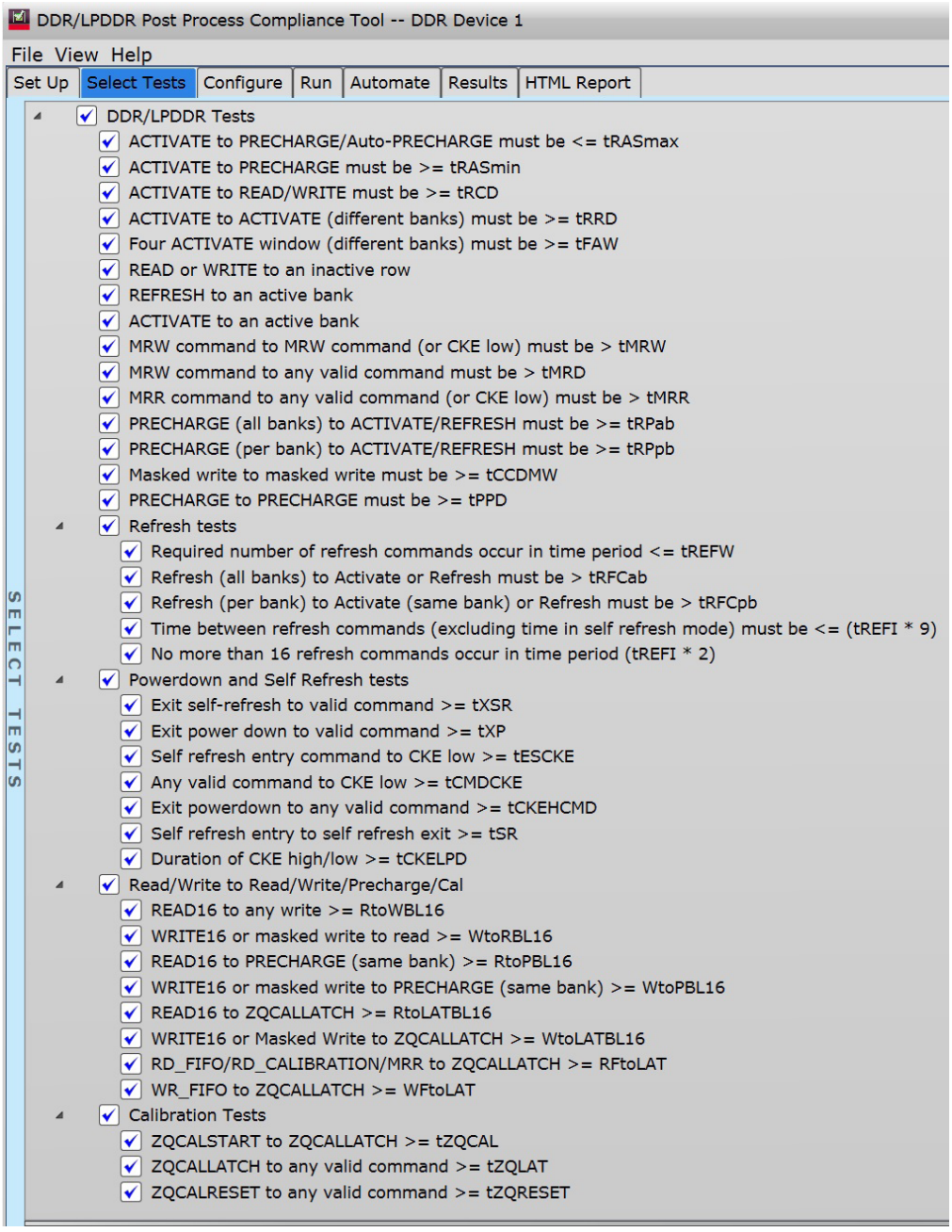


Figure 30. LPDDR4 post process compliance tests from B4661A Option -3FP/TP/NP.

Software (Continued)

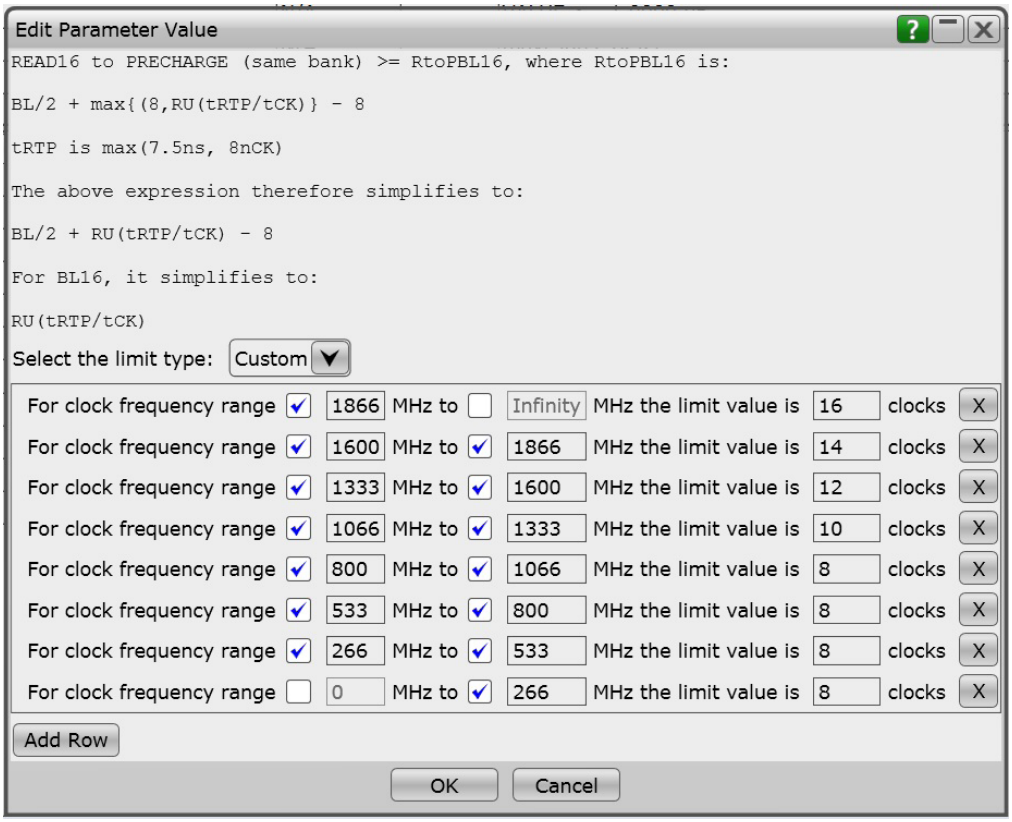


Figure 31. Example LPDDR4 parameter with speed changes, READ16 to PRECHARGE (same bank). The B4661A Option -3FP/TP/NP, post process compliance tool scans the logic analyzer trace capture, calculates the different speed bins, and runs compliance tests on each speed bin.

Software (Continued)

Sample Number	Time	Time	Physical Address	DDR Bus Decode	Cycle Type
				Click here for trigger menu	
-6	-2.480 ns	400 ps		Deselect	Idle
-5	-2.080 ns	400 ps			Idle
-4	-1.680 ns	400 ps		Deselect	Idle
-3	-1.200 ns	480 ps			Idle
-2	-880 ps	320 ps		Deselect	Idle
-1	-400 ps	480 ps			Idle
I▸ 0	0 s	400 ps	0000 0000 0000 0000	Read CS-0 BA-7	Read Command
0.1				Row Address = unknown	*
0.2				Col Address = 0x000	*
0.3				0x00005801	*
0.4				0x0000b303	*
0.5				0x00016216	*
0.6				0x0000cc79	*
0.7				0x00019ce5	*
0.8				0x00003d8f	*
0.9				0x0001730b	*
0.10				0x0001e203	*
0.11				0x0000c006	*
0.12				0x00008c1c	*
0.13				0x00011c6e	*
0.14				0x000130bf	*
0.15				0x0001617a	*
0.16				0x0000c2e6	*
0.17				0x0000818f	*
0.18				0x0000031c	*
1	400 ps	400 ps			Idle
2	800 ps	400 ps			CS=L Cycle
3	1.280 ns	480 ps			Idle
4	1.680 ns	400 ps		CAS-2	CAS-2
5	2.080 ns	400 ps			Idle
6	2.480 ns	400 ps			CS=L Cycle
7	2.960 ns	480 ps			Idle

Figure 32. B4661A Option -2FP/TP/NP, LPDDR4 decode, viewed in Listing window.

The B4661A-2FP/TP/NP option offers a traditional LPDDR decoder for the LA listing window.

Benefits include:

- Complete decode of LPDDR commands with data associated to specific Reads and Writes
- Fastest display of decode (page aware)
- Users can scroll through the listing (or waveform) while computing large traces with the performance software

Configuration Guide and Ordering Information

W6601A includes

- LPDDR4 200-ball, 2 wing BGA interposer
- 200-ball riser for devices under test that have components surrounding the LPDDR4 200-ball DRAM where the surrounding components are too close to install the W6601A without the riser. Riser includes a ground plane. Riser orientation is critical for proper operation
- Qty (16) Single pin headers (part number - W6602-60001)

W6601A requires

- Qty (1) U4208A 61-pin ZIF probe/cable to connect between the left wing of the W6601A and compatible logic analyzer
- Qty (1) U4209A 61-pin ZIF probe/cable to connect between the right wing of the W6601A and compatible logic analyzer
- Qty (1) U4164A logic analyzer module in a chassis with a host controller

Optional for W6601A and W6602A

- 200-ball riser for devices under test that have components surrounding the LPDDR4 200-ball DRAM, where the surrounding components are too close to install the interposer without the riser. Riser includes a ground plane. Riser orientation is critical for proper operation
- The 200-ball riser may be replaced with an optional 200-ball grypper socket (sold separately): **http://www.hsiotech.com/products/released-products/engineering-products/grypper-family**

Recommended configuration for W6601A

Item	Quantity
W6601A LPDDR4 200-ball BGA interposer	1
U4208A 61-pin ZIF probe/cable to connect between the left wing of the W6601A and compatible logic analyzer	1
U4209A 61-pin ZIF probe/cable to connect between the right wing of the W6601A and compatible logic analyzer	1
U4164A logic analyzer module	1
M9502A 2 slot chassis	1
M9537A embedded controller	1
B4661A Option -2FP/2TP/2NP LPDDR decoder	1
B4661A Option -3FP/3TP/3NP compliance analysis	1
B4661A Option -4FP/4TP/4NP performance analysis	1

Configuration Guide and Ordering Information (Continued)

W6602A includes

- LPDDR4 200-ball, rigid BGA interposer
- 200-ball riser for devices under test that have components surrounding the LPDDR4 200-ball DRAM where the surrounding components are too close to install the W6602A without the riser. Riser includes a ground plane. Riser orientation is critical for proper operation
- Qty (16) Single pin headers (part number - W6602-60001)

W6602A requires

- Qty (2) U4207A probe, zero Ω, 34-channel, Soft Touch Pro, direct connect to compatible logic analyzer
- Qty (2) [1] U4164A logic analyzer module in a chassis with a host controller

Recommended configuration for W6602A

Item	Quantity
W6602A LPDDR4 200-ball BGA interposer	1
U4207A probe, zero Ω, 34-channel, Soft Touch Pro, single-ended, 4 x 160-pin direct connect	2
U4164A logic analyzer module	2 [1]
M9505A 5 slot chassis	1
M9537A embedded controller	1
B4661A Option -2FP/2TP/2NP LPDDR decoder	1
B4661A Option -3FP/3TP/3NP compliance analysis	1
B4661A Option -4FP/4TP/4NP performance analysis	1

1. To probe both channel A and B or a single 32 DQ channel, two U4164A modules are required. To probe only one 16 DQ channel, a single U4164A module is required.

Related Products

Item	Description
Modular logic analyzers	
U4164A	36-channel, up to 4 Gb/s state, quad state mode, up to 10 GHz timing, memory depth up to 400 M, AXIe-based logic analyzer module allowing three modules to merge into one time base
Logic analyzer ZIF probe/cables	
U4207A	Probe, zero Ω, 34-channel, Soft Touch Pro, single-ended, 4 x 160-pin direct connect
U4208A	U4208A probe/cable, 61-pin ZIF, from left wing, no RC, 160-pin direct connect to logic analyzer front panel connector
U4209A	U4209A probe/cable, 61-pin ZIF, from right wing, no RC, 160-pin direct connect to logic analyzer front panel connector
Software	
Logic and protocol analyzer software	Required – not licensed; acts as the base software platform
B4661A memory analysis	Required – unlicensed base software
	Licensed options recommended: Options -2FP/2TP/2NP, -3FP/3TP/3NP, and -4FP/4TP/4NP

Related Literature

Publication title	Publication number
W6600 Series LPDDR4 DRAM BGA Interposers - Installation Guide	W6600-97000
Probing Solutions for Logic Analyzers - Data Sheet	5968-4632E
Infiniium 90000 X-Series Oscilloscopes - Data Sheet	5990-5271EN
Capture Highest DDR3 Data Rates Using Advanced Probe Settings on Logic Analyzers - Technical Brief	5991-0799EN
B4661A Memory Analysis Software for Logic Analyzers - Data Sheet	5992-0984EN
U4164A Logic Analyzer Module - Data Sheet	5992-1057EN

www.axiestandard.org

AdvancedTCA® Extensions for Instrumentation and Test (AXIe) is an open standard that extends the AdvancedTCA for general purpose and semiconductor test. The business that became Keysight was a founding member of the AXIe consortium. ATCA®, AdvancedTCA®, and the ATCA logo are registered US trademarks of the PCI Industrial Computer Manufacturers Group.

www.lxistandard.org

LAN eXtensions for Instruments puts the power of Ethernet and the Web inside your test systems. The business that became Keysight was a founding member of the LXI consortium.

www.pxisa.org

PCI eXtensions for Instrumentation (PXI) modular instrumentation delivers a rugged, PC-based high-performance measurement and automation system.

Download your next insight

Keysight software is downloadable expertise. From first simulation through first customer shipment, we deliver the tools your team needs to accelerate from data to information to actionable insight.

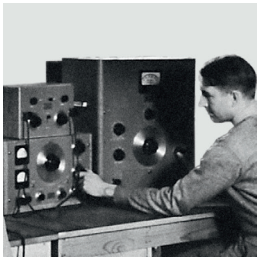
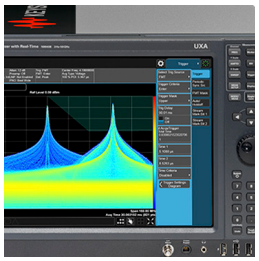
- Electronic design automation (EDA) software
- Application software
- Programming environments
- Productivity software

Learn more at
www.keysight.com/find/software

Start with a 30-day free trial.
www.keysight.com/find/free_trials

Evolving Since 1939

Our unique combination of hardware, software, services, and people can help you reach your next breakthrough. We are unlocking the future of technology.
From Hewlett-Packard to Agilent to Keysight.


myKeysight

myKeysight
www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

http://www.keysight.com/find/emt_product_registration
Register your products to get up-to-date product information and find warranty information.

KEYSIGHT SERVICES
Accelerate Technology Adoption.
Lower costs.

Keysight Services
www.keysight.com/find/service
Keysight Services can help from acquisition to renewal across your instrument's lifecycle. Our comprehensive service offerings—one-stop calibration, repair, asset management, technology refresh, consulting, training and more—helps you improve product quality and lower costs.

CALIBRATION UP TO 10 YEARS WARRANTY
ASSURANCE PLANS

Keysight Assurance Plans
www.keysight.com/find/AssurancePlans
Up to ten years of protection and no budgetary surprises to ensure your instruments are operating to specification, so you can rely on accurate measurements.

Keysight Channel Partners
www.keysight.com/find/channelpartners
Get the best of both worlds: Keysight's measurement expertise and product breadth, combined with channel partner convenience.

www.keysight.com/find/W6601A
www.keysight.com/find/W6602A

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:
www.keysight.com/find/contactus

Americas

Canada	(877) 894 4414
Brazil	55 11 3351 7010
Mexico	001 800 254 2440
United States	(800) 829 4444

Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 11 2626
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Other AP Countries	(65) 6375 8100

Europe & Middle East

Austria	0800 001122
Belgium	0800 58580
Finland	0800 523252
France	0805 980333
Germany	0800 6270999
Ireland	1800 832700
Israel	1 809 343051
Italy	800 599100
Luxembourg	+32 800 58580
Netherlands	0800 0233200
Russia	8800 5009286
Spain	800 000154
Sweden	0200 882255
Switzerland	0800 805353 Opt. 1 (DE) Opt. 2 (FR) Opt. 3 (IT)
United Kingdom	0800 0260637

For other unlisted countries:
www.keysight.com/find/contactus
(BP-9-7-17)

DEKRA Certified
ISO9001 Quality Management System

www.keysight.com/go/quality
Keysight Technologies, Inc.
DEKRA Certified ISO 9001:2015
Quality Management System

Published in USA, December 1, 2017
5992-1461EN
www.keysight.com

KEYSIGHT TECHNOLOGIES